UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/529,539 | 03/29/2005 | Hiroyuki Yoshikawa | 38038 | 4564 |

52054 7590 06/14/2007

PEARNE & GORDON LLP
1801 EAST 9TH STREET
SUITE 1200
CLEVELAND, OH 44114-3108

| EXAMINER | |
|---|---|
| CHOW, CHARLES CHIANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2618 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/14/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/529,539 | YOSHIKAWA ET AL. | |
| | Examiner | Art Unit | |
| | Charles Chow | 2618 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/2/2005 & 3/29/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *02 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## Detailed Action

### Abstract

1. The abstract of the disclosure is objected to because the abstract is too long & containing two paragraphs, with about 200 words. Correction is required. See MPEP§ 608.01(b).

   Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.
   The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. implied language.

### Specification

2. The disclosure is objected to because of the following informalities:

   In line 5 of paragraph 0056, the **"FIG.2"** should be **"FIG.3"**. It is because when signal 131 & signal 132 are displaced from each other in timing, the Fig. 3 shows the characteristic of a sine wave, signal 133. Appropriate correction is required.

### Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   In claims 1, 12, there is no support in the specification, for the particularly pointing out, for which one is for the first modulation input, signal, & for which one is for the second modulation input, signal, in independent claims 1, 12.

For the examination purpose, it is assumed that either modulation input, signal, can be the first or second modulation input, signal.

The dependent claims 2-11 are also rejected due to their dependency upon rejected claim 1.

**Claim Objected**

4. Claim 1 is objected to because of the following informalities:

In claim 1, line 20, the "potion" is assumed to the typographical error of "portion".

Appropriate correction is required.

5. Claim 12 is objected to because of the following informalities:

In line 15 of claim 12, the typographical error for "firs" should be corrected as "first".

Appropriate correction is required.

**Double Patenting**

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 12-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,157,985 B2. Although the

conflicting claims are not identical, they are not patentably distinct from each other because of following reasons:

| Current Application 10/529,539 | US Patent 7,157,985 B2 |
|---|---|
| **Claim 12.** A timing correcting system for a broadband modulation PLL, comprising:<br>a broadband modulation PLL;<br>a measuring portion for demodulating an output signal of the broadband modulation PLL and detecting a value indicating modulation precision; and a measuring unit for demodulating an output signal of the PLL portion and calculating an amplitude value,<br>wherein the broadband modulation PLL comprises a PLL portion containing a voltage controlled oscillator,<br>a frequency divider for dividing the frequency of an output signal of the voltage controlled oscillator,<br>a phase comparator for comparing the output of the frequency-divider with a reference signal, and<br>a loop filter for averaging the output of the phase comparator,<br>a first modulation input portion for inputting a first modulation signal to a first position of the PLL portion,<br>a second modulation input portion for inputting a second modulation signal to a second position different from the first position of the PLL portion on the basis of the modulation data,<br>an operating portion for calculating a timing error on the basis of the amplitude value measured by the measuring unit, and a storage portion for storing a timing set value for controlling the output time of at least one of the first modulation input portion and the second modulation input portion which is calculated on the basis of the timing error, thereby adjusting a modulation timing, the first modulation input portion and the second modulation input portion being controlled so that the timing error is corrected on the basis of the timing set value set in the storage portion. | **Claim 1.** A PLL modulation circuit comprising:<br>a PLL section having: a voltage controlled oscillator;<br>a frequency divider that frequency divides an output signal of the voltage controlled oscillator;<br>a phase comparator that compares an output signal of the frequency divider with a reference signal;<br>a loop filter that equalizes an output of the phase comparator; and<br>an adder that adds an output of the loop filter to a second modulation input signal and sends a result of adding to the voltage controlled oscillator;<br>a first modulation signal generator that, based on a modulation signal inputted, generates a first modulation input signal to input to the frequency divider in the PLL section;<br>a second modulation signal generator that, based on said modulation signal inputted, generates the second modulation input signal to input to the adder in the PLL section;<br>a first calibration signal generator that generates a first calibration signal within a PLL bandwidth to input to the frequency divider in the PLL section;<br>a second calibration signal generator that generates a second calibration signal outside the PLL bandwidth to input to the adder in the PLL section;<br>a demodulator that demodulates an output signal of the voltage controlled oscillator upon adjustment of a modulation level and a time gap between the first calibration signal and the second calibration signal;<br>a low pass filter that blocks a high frequency component of the demodulation signal demodulated in the demodulator;<br>a high pass filter that blocks a low frequency component of the demodulation signal a modulation signal control circuit that compares an amplitude and a phase of an output of the low pass filter and an output of the high pass filter and generates control information; and<br>a modulation signal adjustor that adjusts the first modulation input signal and the second modulation input signal in accordance with the control information. |
| **Claim 13.** A timing error correcting method in broadband modulation PLL comprising:<br>a step of inputting to different two points in PLL modulation data which are opposite to each other in phase;<br>a step of adding modulation signals based on the modulation data;<br>a step of detecting the timing error between the respective modulation signals on the basis of the added modulation signals; and<br>a step of correcting an output timing of at least one of the two-point modulations input to the PLL on the basis of the detected timing error. | The same **Claim 1** above. |
| **Claim 14.** An adjusting method of a radio communication | The same **Claim 1** Above. |

| | |
|---|---|
| device having a broadband modulation PLL for applying modulation to different two points of PLL, comprising:<br>a step of setting a modulation timing of the broadband modulation PLL,<br>wherein the modulation timing setting step comprises<br>a step of inputting to different two points of PLL modulation data which are opposite in phase to each other,<br>a step of outputting a modulation signal of the broadband modulation PLL on the basis of the modulation data,<br>a step of demodulating the modulation signal of the broadband modulation PLL to achieve an amplitude value, a step of detecting the timing error between the respective modulation signals and setting a timing set value into a storage portion provided to the broadband modulation PLL, and<br>a step of correcting a timing of at least one of the two-point modulations input to the PLL. | |
| **Claim 15.** An adjusting method of a radio communication device having a broadband modulation PLL for applying modulation to different two points of PLL, comprising:<br>a step of setting a modulation timing of the broadband modulation PLL,<br>wherein the modulation timing setting step comprises<br>a step of inputting modulation data to different two points of PLL,<br>a step of outputting modulation signals of the broadband modulation PLL on the basis of the modulation data,<br>a step of demodulating a modulation signal of the broadband modulation PLL and detecting a value indicating a modulation degree, a step of detecting the timing error between the respective modulation signals on the basis of a value indicating the modulation precision and<br>setting a timing set value into a storage portion provided to the broadband modulation PLL, and<br>a step of correcting a timing of at least one of the two-point modulations input to the PLL. | The same **Claim 1** Above. |

In the comparison table above, the claims 12-15 of application 10/529,539 are having the equivalent claimed features as the features in claim 1 of US 7,157,985 B2, except using different words for describing the modulation timing control, the derivation of time gap information from the demodulation, associated with the first, second, modulation inputs, for the timing correction, & method, in the first, second, modulation path.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. [ EP 0,408,238 A2] in view of Heck [ US 4,755,774] and Wynn [ US 4,447,792].

**For claim 1,** Johnson et al. [ Johnson ] teaches the A broadband modulation PLL [ the wide band modulation of the frequency synthesizer for a mobile telephone system, Fig. 1, col. 1, lines 3-9] comprising

a PLL portion [ Fig. 1] containing a voltage controlled oscillator 2, a frequency divider [ variable frequency divider 4] for dividing the frequency of an output signal of the voltage controlled oscillator [ voc 2 outputs to divider 4, col. 4, lines 5-7],

a phase comparator [ PSD 6] for comparing the output of the frequency divider 4 with a reference signal [ output of reference divider 10, Fig. 1], and a loop filter for averaging the output of the phase comparator [ low pass filter LPF 14 averaging the output from phase detector PSD 6, Fig. 1 & its corresponding description in the specification] ;

a first modulation input portion for inputting a first modulation signal to a first position of the PLL portion on the basis of input modulation data [ the inputting of R data from 21 to delay Tg 22, as the first modulation input signal to a first position of the PLL, Fig. 1, & its corresponding description in the specification]; and

a second modulation input portion for inputting a second modulation signal to a second position different from the first position of the PLL portion on the basis of the modulation data [ the inputting of R data from 21 to delay Tg 24, as the second modulation input signal to a second different position of the PLL, Fig. 1, & its corresponding description in the specification],

wherein the first modulation signal input to the first position of the PLL portion is added with the second modulation signal at the second position [ the summer 16 adding the first

modulation signal from 22/23 with the second modulation signal from 24, 28/variable divider 4 & 28/30, & its related description in the specification ].

Johnson fails to teach the any one of the first and second modulation input portions inverts the phase of the modulation data, and the inputs the modulation signal to the PLL portion at the time of a modulation timing adjustment to adjust the modulation timing of the first modulation signal and the second modulation signal.

Heck teaches the any one of the first and second modulation input portions inverts the phase of the modulation data [ the inverter 112 inverts one of the modulation input from 22 to modulator 14', second modulation signal from 22 via 25' to vco 18, of the two point modulation, Fig. 8, col. 8, line 60 to col. 9, line 27 & its related description in the specification ], to cancel the modulation components before reaching to phase detector 116; to improve the signal distortion at the synthesizer output [ col. 3, lines 3-9]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve Johnson with Heck's inverter 112, such that the distortion at the output signal could be reduced.

Johnson with Heck fail to teach the inputs the modulation signal to the PLL portion at the time of a modulation timing adjustment to adjust the modulation timing of the first modulation signal and the second modulation signal.

Wynn teaches the inputs the modulation signal to the PLL portion at the time of a modulation timing adjustment to adjust the modulation timing of the first modulation signal and the second modulation signal [ the input of the modulation 16 is inputted at the adjustable time delay 16 connected via 11 to the synthesizer in Fig. 1, for the adjusting the modulation timing of the first modulation to 10 and second modulation to 11, col. 3, lines 1-23, col. 1, lines 44-63, to reduce the distortion with adjustable delay]. Therefore, It would

have been obvious to one of ordinary skill in the art at the time the invention was made to improve Johnson, Heck with Wynn's adjustable delay, such that the distortion could be selectively reduced by utilizing the adjustable delay.

**For claim** 2, Johnson teaches the broadband modulation PLL [Fig. 1, col. 1, lines 3-9], but fails to teach the wherein any one of the first modulating portion and the second modulating portion has an inverter for inverting the phase of the modulation data.

Heck teaches the wherein any one of the first modulating portion and the second modulating portion has an inverter for inverting the phase of the modulation data [the inverter 112 inverts one of the modulation input from 22 to modulator 14', second modulation signal from 22 via 25' to vco 18, of the two point modulation, Fig. 8, col. 8, line 60 to col. 9, line 27 & its related description in the specification ], using the same reasoning in claim 1 above, as the motivation to combine Heck to Johnson.

**For claim** 3, Johnson teaches the broadband modulation PLL [Fig. 1, col. 1, lines 3-9].

Johnson, Heck fail to teach the wherein at least one of the first modulating portion and the second modulating portion has a delay circuit for adjusting the output timing of the modulation signal.

Wynn teaches the wherein at least one of the first modulating portion and the second modulating portion has a delay circuit for adjusting the output timing of the modulation signal [ the one of the input to modulation 16 has the adjustable time delay 16 connected via 11 to the synthesizer in Fig. 1, for the adjusting the modulation timing of the first modulation to 10 and second modulation to 11, col. 3, lines 1-23, col. 1, lines 44-63, to reduce the distortion with adjustable delay], using the same reasoning in claim 1 above, as the motivation to combine Wynn to Johnson & Heck.

**For claim** 4, Johnson teaches the broadband modulation PLL [Fig. 1, col. 1, lines 3-9],

wherein the first modulation input portion generates a frequency-dividing ratio of the frequency divider as the first modulation signal and outputs the first modulation signal to the frequency divider [ the generating of frequency dividing radio at quantiser 28 & outputs the the most significant bit to divider 4, Fig. 1 & col. 4, lines 28-38], and

the second modulation input portion outputs the second modulation signal to the input side of the voltage controlled oscillator [ the second modulation from 22/23 is inputted to the input of VCO 2 via 16, Fig. 1 & its related description in the specification].

**For claims** 9-10, Johnson teaches a modulation system having the broadband modulation PLL [ the wide band modulation for the mobile telephone system , col. 1, lines 3-9]; a radio communication device having the broadband modulation PLL [ the cellular radio device having the wide band modulation, col. 1, lines 3-9].

**Conclusion**

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. **Opsahl et al. [ US 5,903,194]** teaches the frequency synthesizer has modulation input including a delay 130 which is subtracted from its input 138 via selection in multiplex 134, 70, Fig. 5, Fig. 6 & its related description in the specification].

B. **Flugstad et al. [ US 4,810,977]** teaches the PLL with adjustable delay 31, Fig. 2 & its related description in the specification].

C. **Gossmann et al. [ US 2001/0036,240 A1]** teaches the phase delay 10/22, in two point modulation [ Fig. 2 & its related description in the specification].

D. **Chang [ US 6,160,456]** teaches the PLL with first delay array 271 in figure in cover page & its related description in the specification].

E. **Groe [ US 7,061,341 B1]** teaches the two point modulation [ Figure in cover page & its related description in the specification].

F. **Hietala [ US 5,166,642]** teaches the delay arrangement for the multiple accumulators for a synthesizer [ Figure in cover page & its related description in the specification].

G. **Trichet et al. [ US 6,211,747 B1]** teaches the two point modulation in a frequency synthesizer including detecting vco input voltage [ Figure in cover page & its related description in the specification].

H. Other references are also considered. They are: **Hirano [ US 2006/0202,774 A1], Nishimura et al. [ US 2002/0105,389 A1], Yoshikawa et al. [ US 2005/0232,385 A1], Matsuyoshi et al. [ US 7,046,972 B2], Grewing et al. [ US 2005/0046,488 A1], Grewing et al. [US 2004/0192,231 A1], Hammes et al. [ US 2004/0036,539 A1], Nienaber [ US 4,611,230], Salvi [ US 5,557,244], Filiol et al. [ US 6,515,553 B1], Dent [ US 5,983,077], Linebarger et al. [ US 6,141,394].**

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR

only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow CC.

June 1, 2007.

EDWARD F. URBAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600